Multichannel Pattern Generator BPG 4x32G

Key Features

- **Broadband Pulse Pattern Generator for Test and Measurement Applications**
- **Gap-Free Operation at Data Rates between 1 Gbps and 32 Gbps**
- **PRBS and User Programmable Pattern of Variable Length up to 4*256 MBit**
- **Independently Adjustable Output Level for Each Channel**
- **Jitter-transparent for Jitter Tolerance Testing**
- **Operation via Front Panel or USB-Interface**
- **Optionally Available:**
  - **Independently Adjustable Delay of $\pm 35\,ps$ for Each Output Channel**
  - **Integrated Clock Generator**
  - **Extended Output Swing up to $2\,V_{pp}$ Single-ended**

This wideband tuneable 4-channel pulse pattern generator provides hardware-based pseudo random binary sequences and memory-based user programmable bit patterns. The four output channels run synchronously but are independently adjustable. An internal clock source, adjustable output amplitude and various pattern modes make the instrument adapted to a wide field of test and measurement applications. Fast signal transitions times below 15 ps typically and a RMS jitter under 1 ps assure good signal quality. In combination with the Error Analyzer SBF 28G or SBF 44G the pattern generator forms a complete bit error rate test set.

Clock Source

The clock source determines the time base for operation. All the output signals are derived from it. The pattern generator is operated with a clock signal of half the output data rate, i. e. with a clock signal of 16 GHz the instrument generates output patterns at 32 Gbps. Optionally the instrument is available with a full-clock input and internal divider.

External Clock

The clock signal connected to the instruments *Clock Input* is used as system clock. The clock input is jitter-transparent and the instrument follows even abrupt frequency changes of the externally attached signal. The optionally available input clock divider allows to operate the pattern generator in full and half clock

mode, e. g. to generate a 32 Gbps output signal a 32 GHz or a 16 GHz clock signal can be connected.

Pattern

PRBS

Hardware generated pseudo random binary sequences of length between $2^7 - 1$ and $2^{31} - 1$ can be selected as pattern data.

PRBS	2^n-1, n=7, 9, 11, 15, 23, 31	
PRBS	Polynomial	Specification
2^7-1	X^7+X^6 +1	
2^9-1	X^9+X^5 +1	CCITT O.153/ITU-T O.153
2^{11}-1	$X^{11}+X^9$ +1	CCITT O.152/ITU-T O.152
2^{15}-1	$X^{15}+X^{14}$ +1	CCITT O.151/ITU-T O.151
2^{23}-1	$X^{23}+X^{18}$ +1	CCITT O.151/ITU-T O.151
2^{31}-1	$X^{31}+X^{28}$ +1	CCITT O.150/ITU-T O.150

Additional pseudo random binary sequences of length up to $2^{21} - 1$ can be generated by loading the corresponding pattern data into the pattern memory of the generator[1].

In PRBS mode there is a phase lag of one quarter of the length of the pseudo random sequence between each pair of output channels A-B, B-C and C-D to fulfill CCITT recommendations after 4 to 1 multiplexing.

Data

Arbitrary user pattern data up to a maximum length of 4*64 MBit can be generated. The pattern length can be set in steps of 128 bits. The programmed bit sequence is generated periodically. Additionally the pattern memory can be split in 2 or 4 parts to toggle synchronously between different waveforms. Optionally the pattern generator is available with an extended pattern memory of 4x128 MBit or 4x256 MBit.

Pulse Format

NRZ

Non-return to zero pulse format. The output signal remains at the low or high level according to the level of the selected bit pattern for the entire period of the selected clock source.

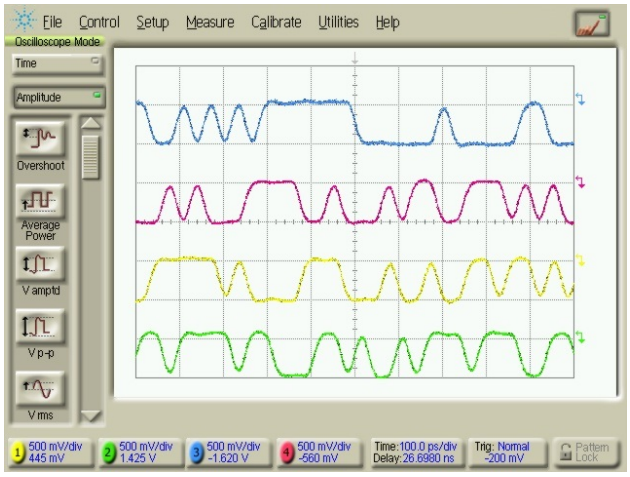


Figure 1: Pulse pattern of the four output signals at 32 Gbps

Output Modes

Pulse Pattern Mode

The selected bit pattern is repeated periodically.

Alternate Subpattern Mode

In this mode two subpatterns A and B of the same length can be generated alternately. The AUX input can be used to toggle synchronously between patterns A and B. The alternate subpattern mode can also be used to generate repetitive signal bursts.

Data Polarity

The polarity of the output signals can be set to normal or inverted. If the polarity is set to inverted the low and high level bits are interchanged. In PRBS mode normal polarity corresponds to the PRBS pattern definitions according to CCITT specifications.

Output Amplitude

The output amplitude is adjustable between 0.35 V_{pp} and 0.55 V_{pp}.

[1] depending on the pattern memory size of the device

Bit Shift

In PRBS mode the bit shift functionality allows to delay the output signal by n bits ($0 \leq n \leq 16777216$) to compensate for cable delays or to synchronize the two subchannel patterns at specific bit positions.

Figure 2: Output pattern delayed by 3 bits

Delay

Each channel has an integrated timing delay of $\pm 10\,ps$ that is independently adjustable in steps of 1 ps. Optionally the pattern generator is available with an extended delay of $\pm 35\,ps$ per channel.

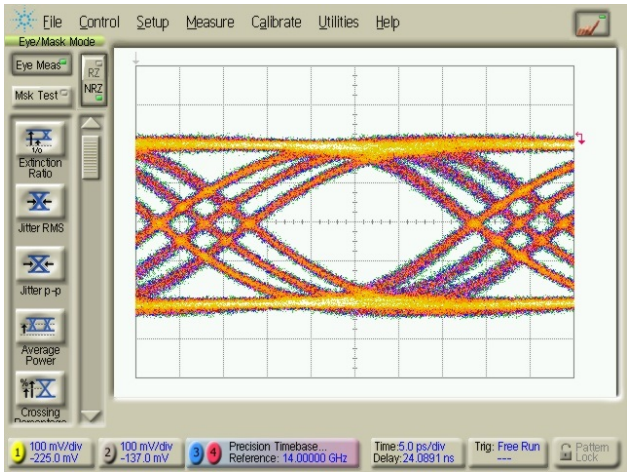


Figure 3: Example of output signal at 28 Gbps delayed in steps of 5 ps

Error Insertion

The error addition allows to add errors to the output data stream. The error addition can be turned on and off separately for each channel.

Programmable Error Addition

Error rates between 10^{-4} and 10^{-11} and single error mode are selectable. Exactly one bit is inverted, e. g. if the error rate 10^{-9} is selected, one out of 10^9 bits will be inverted.

Error Input

The error input accepts a TTL signal. With every transition of the signal connected to the error input an error is added to the output data stream. The maximum toggle frequency at the error input is 100 kHz.

Trigger Signals

Trigger Output

The trigger output provides a divided clock signal or a pattern synchronous trigger signal.

Clock Output

The clock output provides a clock signal of half the system clock frequency.

Aux Input

In the alternate subpattern mode the AUX input can be used to toggle synchronously between two subpatterns.

Jitter Insertion

When the external clock input is used the pattern generator follows exactly the externally connected frequency. By modulating the external clock source jitter-modulated data signals can be generated. Optionally the BPG 4x32G is also available with an internal time delay. By applying a modulation signal to the delay control input various shapes of signal jitter can be generated.

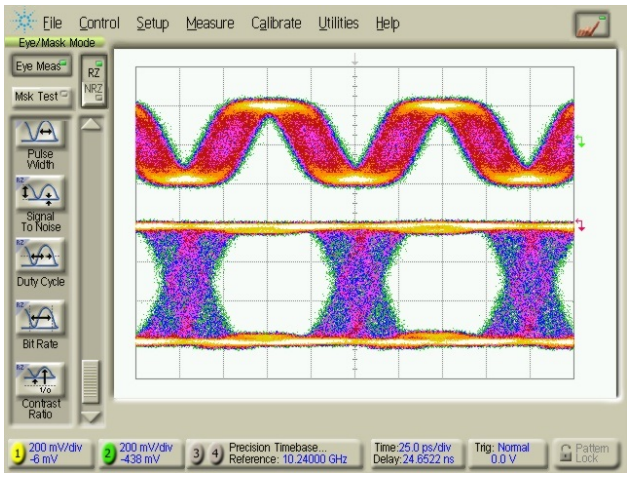


Figure 4: Jitter modulated with sine-wave: Clock Input and Data Output Signal at 10.24 Gbps

Front Panel Controls

All main instrument settings can be changed using the control buttons on the front panel. The device parameters are accessible through an intuitive menu structure that is displayed on the front LCD.

Graphical User Interface

The graphical user interface allows to change all device settings, program the user pattern and set the internal clock rate by simple mouse-clicking. The last settings are automatically saved when power is turned off.

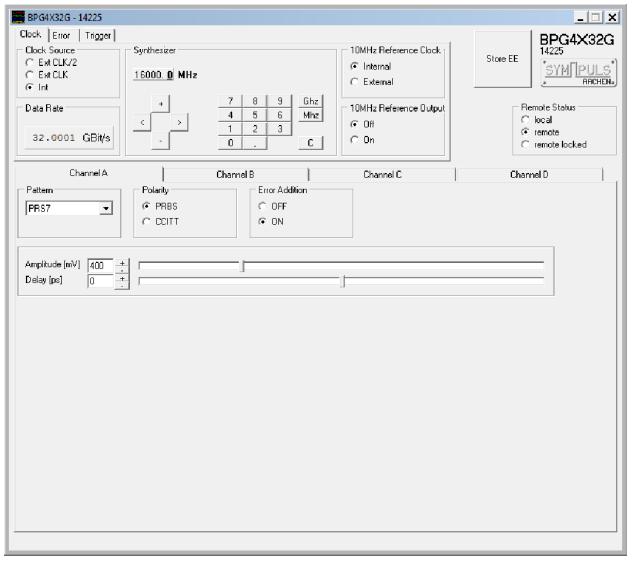


Figure 5: Graphial User Interface of the Operating Software

SCPI Remote Control

The pattern generator can be remotely controlled via SCPI commands, a standardized instruction set for controlling and programming measurement instruments. The SCPI commands are transfered to the instrument in ASCII text format and may be generated using any programming language and development environment.

Connectors

Front Panel Connectors

On the front panel the following signals are accessible:

- Clock Input
- Complementary Data Outputs for Each Channel
- Complementary Clock Outputs
- Trigger Output

Rear Panel Connectors

The rear panel contains the mains plug and the USB 2.0 interface. Additional signal connectors are:

- 10 MHz Reference Input (with internal clock only)
- 10 MHz Reference Output (with internal clock only)
- Error Input
- AUX Input

Options

Extended Pattern Memory

The pattern generator BPG 4x32G is also available with an extended pattern memory of 128 MBit or 256 MBit per channel.

Full-Clock Input

The integrated divider allows to connect clock signals of the full output data rate, i. e. 32 GHz for 32 Gbps output data signals. The clock input can be switched over from full-clock mode to half-clock mode.

Internal Clock

The internal quartz controlled clock generator provides clock signals in the range from 250 MHz to 16 GHz with a frequency resolution of 100 kHz.

A 10 MHz reference clock signal can be applied to the reference clock input on the instruments rear panel. This clock signal is used as reference for all timing parameters.

The 10 MHz reference clock output signal can be used to synchronize the time base of other instruments to the time base of the pattern generator.

Extended Output Amplitude

Optionally the generator is available with extended output levels of up to $2\,V_{pp}$ single-ended as well as crosspoint an DC-offset control. Fast signal transitions with rise-times (20%-80%) typically <12 ps.

Extended Delay

The extended delay permits to delay each channel independently by $\pm 35\,ps$.

GPIB IEEE-488.2 Interface

In addition to its USB interface the pattern generator is available with a GPIB interface. The active interface can be selected in the instruments setup menu.

56 Gbps outputs

The instrument is also available with up to two output channels operating at data rates between 1 Gbps and 56 Gbps. The 56 Gbps output channels are generated by multiplexing two of the instruments sub-channels.

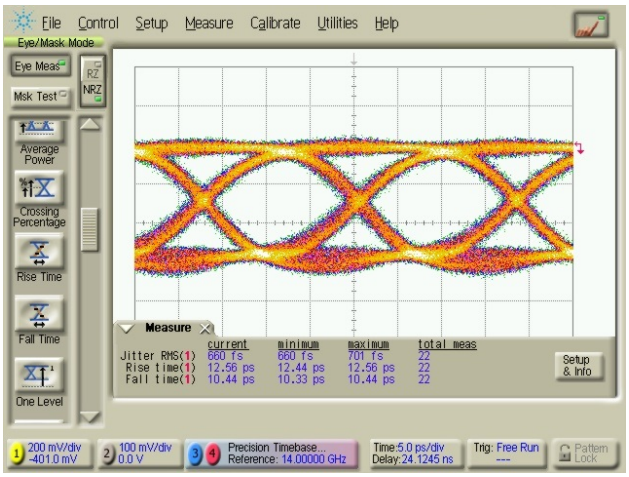


Figure 6: 56 Gbps Output Eye

Technical Specifications

Pulse Pattern Generator BPG 4x32G	
External Clock	
Frequency Range	500 MHz ... 16 GHz (External Clock Rate = (Data Rate)/2) 6-digit frequency display
Impedance	$R_i = 50\,\Omega$, $\lvert r\rvert < 0,2$
Input Amplitude	$U_i = 0,5 \ldots 1,0\,V_{pp}$,
Connector	50 Ω 2.92 mm (K)
Pattern Generation	
Data Format	Non-return to zero
Data Rate	According to Input Clock, 1 Gbps ... 32 Gbps
PRBS	$2^{31}-1$, $2^{23}-1$, $2^{15}-1$, $2^{11}-1$, 2^9-1, 2^7-1
Pattern Memory	67 108 864 Bit (per channel)
Programmable Pattern Length	$128 * m$ Bit $(m = 1, 2, 3, \ldots, 2^{20})$
Long user patterns only programmable via the instruments USB interface	
Data Outputs	
4 channels with complementary data outputs NRZ and /NRZ, DC-coupled	
Amplitude	$0\,V/U_{peak}$, $-0.55\,V \leq U_{peak} \leq -0.35\,V$ (±0.1 V)
Rise/Falltime (20%-80%)	< 17 ps
Jitter (rms)	< 1 ps (at maximum amplitude)
Duty Cycle	50% ±2.5%
Data Polarity	Normal or Inverted Logic
Internal Delay	$\pm 10\,ps$, independently adjustable for each channel
Impedance	$R_i = 50\,\Omega$, $\lvert r\rvert < 0.2$
Connector	50 Ω 2.92 mm (K), $\lvert r\rvert < 0.2$
Clock Outputs	
Complementary clock outputs (Bit Rate)/2 and /(Bit Rate)/2, AC-coupled	
Amplitude	$0.5\,V_{pp} \pm 0.1\,V$
Rise/Falltime (10%-90%)	< 15 ps
Data to Clock Skew	±10 ps
Connector	50 Ω 2.92 mm (K)
Trigger Output	
Trigger Modes	1. Bit Rate/16 2. Word Frame Trigger (Data Pattern Synchronous Trigger)
Amplitude	$(-0.4\,V \pm 0.1\,V)/0\,V$, DC Coupled
Connector	50 Ω SMA, $\lvert r\rvert < 0.2$

Pulse Pattern Generator BPG 4x32G	
Error Insertion	
Programmable Error Addition	Single, $10^{-4}, 10^{-5}, \ldots, 10^{-11}$
Error Input	TTL Input, Maximum Error Frequency 100 kHz
General Information	
Interface	Operation via Front Panel or High Speed USB Data Transfer Rate up to 10 MByte/s
Software	Graphical User Interface for Operation and Pattern Programming
Dimensions	10” Desktop W x H x D = 462 x 178 x 480 mm^3
Weight	approx. 9 kg
Power Supply	115 V/230 V/50-60 Hz/175 VA

Options

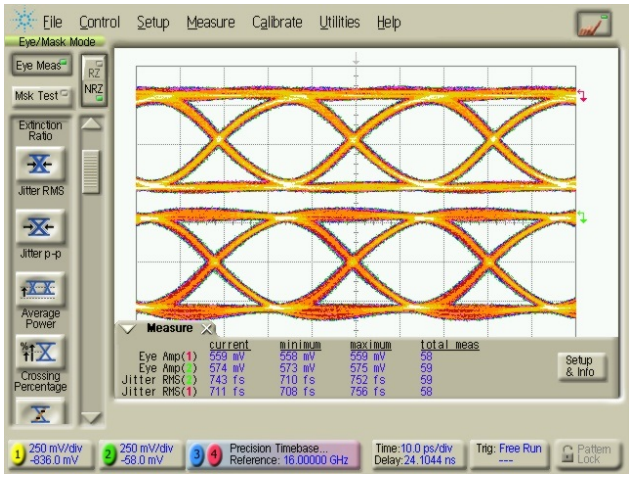
Option 1: Extended Memory 4x128 MBit	
Pattern Memory	134 217 728 Bits
Patten Length	$256 * m$ Bits, $(m = 1, 2, \ldots, 2^{20})$
Option 2: Extended Memory 4x256 MBit	
Pattern Memory	268 435 456 Bits
Patten Length	$256 * m$ Bits, $(m = 1, 2, \ldots, 2^{21})$
Option 3: Full-clock Input	
Input Frequency	1 GHz ... 32 GHz (External Clock Rate = Data Rate) *Full-clock* and *half-clock* input selectable
Option 4: High-power Output Driver	
Data Rate	1 Gbps ... 32 Gbps
Amplitude	$1.0\,V_{pp} \ldots 2.0\,V_{pp}$ single-ended into 50 Ω
DC-Offset	$0\,V \ldots 1.25\,V$
Rise-/Falltimes (20%-80%)	$<$ 12 ps
Crossing	30% ... 70%
Option 5: Internal Clock	
Quartz controlled clock generator	
Frequency Range	250 MHz ... 16 GHz
Frequency Resolution	100 kHz
10 MHz Reference Input	$U_i = 1\,V_{pp} \ldots 3\,V_{pp}$ 50 Ω SMA, AC-coupled
10 MHz Reference Output	Amplitude $1.5\,V_{pp}$ 50 Ω SMA, AC-coupled
Option 6: Extended Delay	
Internal Delay	$\pm 35\,ps$, independently adjustable for each channel
Option 7: Fast 56 Gbps Multiplexed Output Channel	
Data Rate	1 Gbps ... 56 Gbps, gap-free
Data Outputs	Complemetary data outputs NRZ and /NRZ, DC-coupled
Amplitude	$0.4\,V_{pp} \ldots 0.6\,V_{pp}$ Single-Ended,
Rise-/Fall-Times (20 %/80 %)	$<$ 12 ps
Jitter (rms)	$<$ 750 fs[2]
Duty Cycle	50%, Adjustable
Connector	50 Ω 2.4 mm
Option 8: GPIB IEEE-488.2 Interface	
Interface	GPIB IEEE-488.2
Data Transfer Rate	up to 1.5 MByte/s

[2] For input clock signal with Jitter(rms)<500 fs

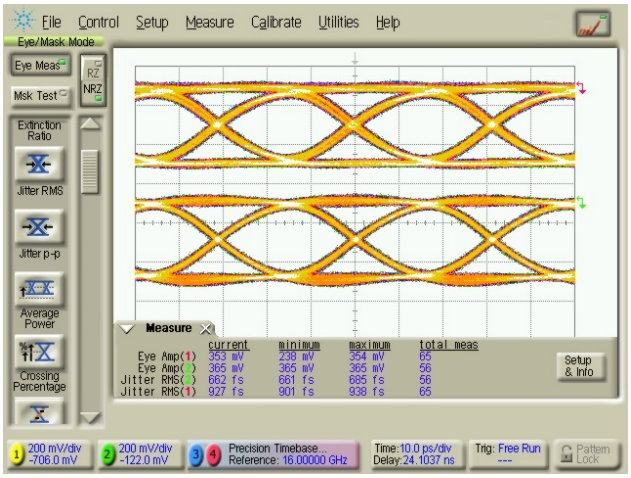
Output Signals

All oscillograms in this section were taken using the Agilent 86100B sampling oscilloscope and the sampling module 86118A (70 GHz cut-off frequency).

Typical Output Waveforms



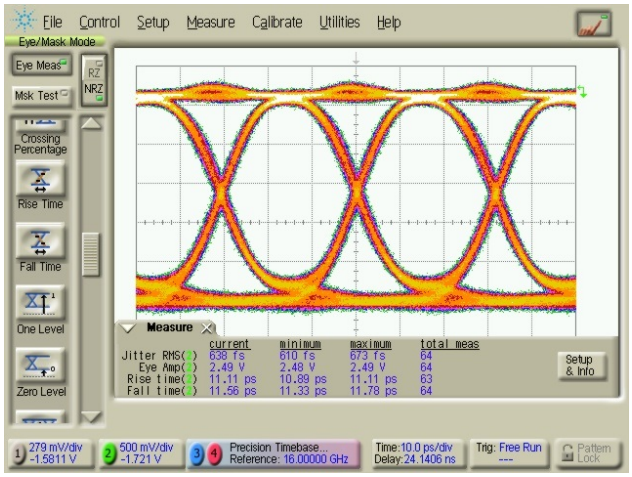
(a) Output Signal at Maximum Amplitude



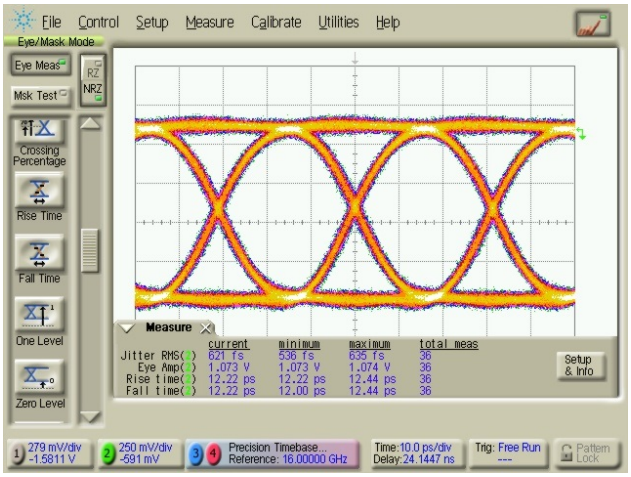
(b) Output Signal at Minimum Amplitude

Figure 7: Jitter and Transition Times at 32 Gbps

Option 5: Extended Output Levels



(a) Output Signal at Maximum Amplitude



(b) Output Signal at Minimum Amplitude

Figure 8: Data Outputs at 32 Gbps with Extended Output Levels

Ordering Information

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Included in delivery:

BPG 4x32G

- Mainframe
- User Manual, USB Cable
- CD-ROM with Device Drivers and Operating Software

The instrument is produced by SYMPULS in Germany.
We offer a reliable service and 24 month warranty.