Pattern Receiver SBF 3000

Key Features

Self-synchronizing Pattern Receiver with Error Counter

Gap Free Coverage of Bit Rates between 50 Mbps and 3 Gbps

Integrated Data Threshold and Clock Phase Adjustment

Operation via Front Panel or via USB-Port

Optionally available:

- **Internal Clock Recovery Circuit**

Brief Description

The Pattern Receiver SBF 3000 is used to detect errors contained in a data stream. In combination with the Pattern Generator PAT 3000 it forms a complete measurement set for bit error rate testing (BERT).

Synchronous clock and data signals are needed to perform a measurement. The *Clock Recovery* option allows to recover the required clock signal from the connected data signal. Six different pseudo random binary sequences (PRBS) of length 2^7-1, 2^9-1, $2^{11}-1$, $2^{15}-1$, $2^{23}-1$ and $2^{31}-1$ structured according to the CCITT standard can be analysed using bitrates between 50 MBit/s and 3 GBit/s.

Two different error rates can be measured: Errors per Bit and Errors per Time. The time interval for error measurements can be choosen between 10^5 and 10^{14} bit periods for the Error/Bit measurement and between 10^{-5} und 10^4 seconds for the Error/Time measurement.

The integrated data threshold and clock phase adjustment allows a detailed analysis of the connected data signal.

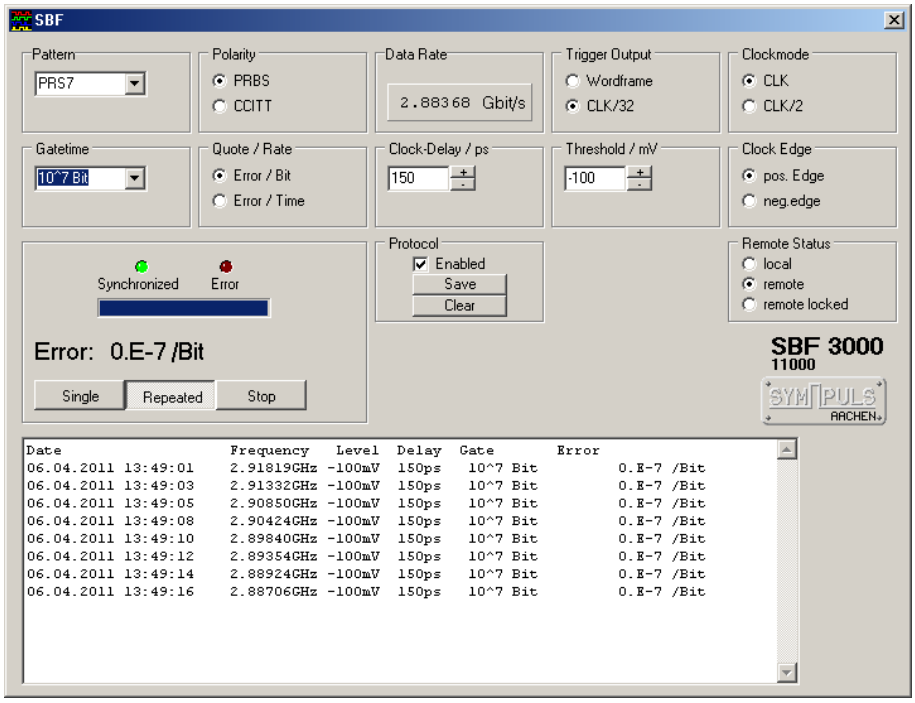
The instrument is operated via push buttons on the front panel. The results are displayed on the front panel display. Additionally the device can be remotely controlled via its USB-interface. An easy-to-use graphical user interface is included in the supplied software.

Technichal Specifications

SBF 3000	
Synchronisation	50 Mbps . . . 3 Gbps (with External Clock) Phase Shifting of $-150 \ldots 200$ ps through Adjustable Data Delay Automatic Frame Synchronisation Synchronisation LED
Clock Input	Clock or Clock/2 , $U_i = 0,3 \ldots 1,0\, V_{pp}$, 50 Ω SMA, AC Coupled, $\lvert r\rvert < 0,2$ for Clock Input the Active Pulse Edge is Selectable
Pattern	PRBS $2^{31}-1$, $2^{23}-1$, $2^{15}-1$, 2^7-1
Data Input	NRZ, Pos./Neg. Logic Selectable, $U_i = 0,3 \ldots 0,8\, V_{pp}$, 50 Ω SMA, $\lvert r\rvert < 0,2$ Adjustable Threshold, Display of Data Balance: LED-Display of 1/0 Distribution after Decision Unit
Clock Output	Clock or Clock/2 according to Input Clock, $0,4\, V_{pp}$, 50 Ω SMA
Trigger Output	Selectable: 1. Clock/16 2. Word Frame Trigger $0,4\, V_{pp}$, AC Coupled 50 Ω SMA, $\lvert r\rvert < 0,2$
Error Counter	Error Rate Measurement (Resolution 6 Digits: 5 Mantissa, 1 Exponent): 1. Error/Time: $10^7 \ldots 10^{-4}$/ s Gate Time: $10\,\mu s \ldots 10.000\, s$ 2. Error/Bit: $10^{-3} \ldots 10^{-14}$ Gate Time: $10^5 \ldots 10^{14}$ Clock Periods Single or Repetitive Measurement Error Display: LED
Interface	Hgh Speed USB Max. Data Transmission Rate 2 MByte/s
Software	Graphical User Interface for Operation
Dimensions	10” Desktop W x H x D = 256 x 80 x 264 mm
Weight	approx. 3 kg
Power Supply	115 V/230 V/50-60 Hz/20 VA
Optionally Available	
Option 1	Internal Clock Recovery for Data Rates from 50 Mbps to 3 Gbps

Graphical User Interface

All instrument settings can be changed via an easy-to-use graphical user interface on your PC. The measurement results are displayed and can be saved to a file.



Graphical User Interface of the Operating Software

Ordering Information

Included in delivery:

- SBF 3000
- User Manual, USB Cable
- CD-ROM with Device Drivers and Operating Software

The instrument is produced by SYMPULS in Germany.
We offer a reliable service and 24 month warranty.